REMARKS / ARGUMENTS

Claims 21-53 remain pending in this application. No claims have been canceled. New claims 44-53 have been added.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the priority document.

Information Disclosure Document

On page 5 of the PTO 1449 Forms filed with the Information Disclosure Statement on April 27, 2006, references AB - AJ have not been initialed by the Examiner. Applicants respectfully request the Examiner to indicate consideration of these documents. A copy of page 5 is enclosed for the Examiner's convenience.

Title

The Title of the invention has been rewritten in a more descriptive form as required by the Examiner.

Claim Objections

Applicants appreciate the Examiner's pointing out minor errors in the claims. Claims 37 and 38 have been amended as suggested by the Examiner. However,

claims 22-25 and claim 35 are not believed to require any amendment. Independent claim 21 is directed to "A storage system". Therefore, it is submitted that the dependent claims should refer to "The storage system" as opposed to "The storage device", as suggested by the Examiner. As this may have been an inadvertent error by the Examiner, the claims have been amended to recite "The storage system".

Furthermore, with respect to claim 35, although the word "at" appears twice consecutively, it is submitted that the language is appropriate under the circumstances. In particular, this portion of the claim is directed to data received at at least one of the first interface adaptors.

The Examiner is hereby invited to contact the undersigned with any questions.

35 U.S.C. § 103

Claims 21-43 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hubis et al (U.S. Patent No. 6,343,324) in view of Kuchta et al (U.S. Patent No. 6,014,319). These rejections are traversed as follows.

The present invention is directed to a storage system having disk drives, at least one logical volume configured by the disk drives, a processor adaptor having a processor and controlling to store data which are sent from one or more host computers, and a plurality of first interface adaptors as recited in the claims. According to the present invention, since the processor adaptor is recited to have a processor, while the interface adaptors do not, each processor can be used more efficiently. On the other hand, if the interface adaptors each had their own

processor, each such processor could only execute operations run within each interface adaptor. Therefore, if the I/O access to a first interface adaptor is much greater than that to a second interface adaptor, a bottleneck can occur in the processor of the first interface adaptor thereby degrading data performance of the storage system. At the same time, the processor in the second interface adaptor is not being fully utilized. This also deteriorates the data transfer performance of the storage system.

None of the cited references disclose or suggest these features of the pending claims. Hubis et al disclose a method for accessing a logical volume from a host computer using a World Wide Name (WWN). The processor controls access based on a table describing the relationship between a LUN and host ID (for example, WWN) (see column 8, lines 28-37).

Kuchta et al disclose I/O modules 209-212 that communicate with one or more host computer systems over a local area network or other medium and/or communicate with storage devices located in drawers 104-107. The I/O communication modules 209-212 handle the transfer data between drawer 102 and the storage devices (see column 5, lines 32-45).

However, neither Hubis et al nor Kuchta et al disclose or suggest the features of the present invention recited above. The Examiner appears to equate (a) the first interface adaptor and the second interface adaptor of the claimed invention to the I/O processor 184, 185 in Fig. 2A of Hubis et al, (b) the processor adaptor of the claimed invention to the processor 180 in Fig. 2A of Hubis et al, and (c) the memory

adaptor of the claimed invention to the data cache memory 186 in Fig. 2A of Hubis et al. Since Applicants believe that the correspondence between the claimed invention and Hubis et al cannot be maintained based upon the assertions set forth above, each assertion will now be discussed in more detail.

With respect to the first interface adaptor and the second interface adaptor of the claimed invention with respect to I/O processor 184, 185 in Fig. 2A of Hubis et al, Applicants point out that the I/O processor 184, 185 of Hubis et al are dedicated to process I/O access (see column 11, lines 22-25 and lines 30-36). On the other hand, the first interface adaptor and the second interface adaptor of the claimed invention do not have a processor since the processors are aggregated to the processor adaptor.

With respect to the processor adaptor of the claimed invention, Applicants wish to point out that the processor 180 of Fig. 2A of Hubis et al coordinates the activities of all of the I/O processors 184, 185 and handles scheduling of tasks including read and write tasks, as well as error handling (see column 16, lines 6-9). On the other hand, the processor adaptor of the claimed invention sends instructions concerning data transfer based on the control information. The processor 180 of Hubis et al does not have the function an that claimed for the processor adaptor of the present invention.

With respect to the memory adaptor of the claimed invention, Applicants point out to the Examiner that the data cache memory 186 in Fig. 2A of Hubis et al buffers data to be sent between the host computer 101 and disk drives 108 (see column 15,

lines 63-66). This cache memory does not store control information. However, the memory adaptor of the claimed invention has a control information memory module 127 in order to store control information. New dependent claims have been added specifically directed to this point.

Furthermore, the Examiner suggests that Kuchta et al disclose a plurality of processor adaptors, citing column 5, lines 47-48, Fig. 2B, elements 213-216. Applicants assume that the Examiner intended to refer to I/O modules 209-212 which are disclosed at column 5, lines 47-48. Nevertheless, it is submitted that these I/O modules do not correspond to the claimed processor adaptor, but correspond to the first interface adaptor and second interface adaptor. Therefore, it is submitted that the attempt at combination of references fails to disclose or suggest the presently claimed invention. As such, it is submitted that the pending claims patentably define the present invention over the cited art.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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